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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional): 10031133-1

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on 6/28/07 VIA EFS WEB

Signature: /MJT/

Typed or printed name: Michael J. Tempel

Application Number	Filed
10/820,484	April 8, 2004
First Named Inventor	
Michael G. Kelly	
Art Unit	**Examiner**
2826	Andujar, Leonardo

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

- [ ] applicant/inventor.
- [ ] assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)
- [ ] attorney or agent of record. Registration number _____
- [X] attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34: 41,344

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June 28, 2007
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

- [ ] *Total of 1 forms are submitted.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:	Group Art Unit: 2826
Michael G. Kelly	Examiner: Andujar, Leonardo
Application No.: 10/820,484	Docket No.: 10031133-1
Filed: April 8, 2004	Confirmation No.: 7400

For: **Thermal Dissipation In Integrated Circuit Systems**

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SMITH FROHWEIN TEMPEL
GREENLEE BLAHA LLC
Customer Number 35856

Sir:

Claims 1-21 are pending and the subject of this Pre-Appeal Brief Request For Review.

Claims 1-9 and 21

Claims 1-9 and 21 are rejected under 35 U.S.C. § 103(a) over Hideshima (U.S. 5,143,865) in view of Wu (U.S. 2003/0067057). In the rejection of independent claim 1, the Examiner has stated that Hideshima "does not disclose a top side thermal dissipation metallization" (see page 2, ¶ 3, line 5, of the Office Action dated May 7, 2007). In an effort to make-up for this failure of Hideshima's disclosure, the Examiner has relied on the teachings of Wu. In particular, the Examiner has taken the position that (see page 2, ¶ 3, lines 5-10, of the Office Action dated May 7, 2007):

> . . . Nevertheless, Wu (e.g. fig. 3A) shows a die a topside thermal dissipation metallization 21. This type of embodiment allows the heat generated from a semiconductor chip to be quickly dissipated through a die pad of the lead frame after the semiconductor chip is attached to the die pad, so as to improve overall heat dissipating efficiency of the semiconductor package (pp 0009). . . .

In FIG. 3A, Wu shows a semiconductor package 2 that includes a semiconductor chip (or die) 23 that is bonded to a lead frame and is encapsulated by an encapsulant 25. The lead frame has leads 222 and a die pad 21, which are formed by a half-etching process (see ¶ 34, line 5 and lines 15-20). Solder bumps 24 bond contact pads on the active surface 230 of the semiconductor chip 23 to the leads 222, and a non-conductive thermal adhesive 212 bonds the active surface 230 of the semiconductor chip 23 to the die pad 21.

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Date: 6/28/07 _____
Signature –Michael J. Tempel

Contrary to the Examiner's statement, the die pad 21 does not constitute a top side thermal dissipation metallization that is supported on the top side of the semiconductor chip 23. First, the die pad 21 is not a "metallization" as defined in the specification. On page 4, lines 3-4, the specification recites that "As used herein, the term 'metallization' refers to single-layer metal film or a multi-layer metal film formed in or on an integrated circuit." The die pad 21 does not constitute a single-layer metal film or a multi-layer metal film. Instead, the die pad 21 is an integral component of a package lead frame that is adhesively bonded to the semiconductor chip 23 only when the semiconductor chip 23 is mounted in the package 2 (see FIG. 2B, which shows the die pad 110 as an integral component of the lead frame 10). Thus, one skilled in the art at the time the invention was made would not have considered the die pad 21 to be a "thermal dissipation metallization" as recited in claim 1. Second, there is no reasonable interpretation of the word "supported" that could read on the die pad 21, which operates to stop the semiconductor chip 23 from moving downwardly during the process of reflowing the solder bumps 24 (see, e.g., ¶ 34, lines 10-15; see also ¶ 31). Third, in Wu's disclosure, bonding pads are the only elements that are supported on the top side of the semiconductor chip 23 (see, e.g., FIG. 3A). One skilled in the art at the time the invention was made reasonably would infer from this disclosure, that the top surface of the semiconductor chip 23 is devoid of any type of structural elements designed to dissipate heat through the adhesive 212 and the die pad 21.

In summary, neither Hideshima nor Wu teaches anything about a die that has a top side supporting top side thermal dissipation metallization as recited in claim 1. Therefore, the combination of Hideshima and Wu cannot possibly teach or suggest the invention defined by independent claim 1. For at least this reason, the Examiner's rejection of independent claim 1 under 35 U.S.C. § 103(a) over Hideshima and Wu should be withdrawn.

The rejection of claim 1 under 35 U.S.C. § 103(a) over Hideshima in view of Wu also should be withdrawn because this rejection relies on an impermissible combination of the teachings of Hideshima and Wu. The Examiner has stated that (see page 3, ¶ 3, line 10 to page 4, ¶ 3, line 2, of the Office Action dated May 7, 2007):

> . . . It would have been obvious to one of ordinary skill in the art at the time the invention was made to form a top side thermal dissipation metallization layer as disclosed by Wu to allow the heat generated from a semiconductor chip to be quickly dissipated through a die pad of the lead frame after the semiconductor chip is attached to the die pad, so as to improve overall heat dissipating efficiency of the semiconductor package as suggested by Wu.

This rationale, however, does not establish a *prima facie* case of obviousness under 35 U.S.C. § 103 (see MPEP § 706.02(j)) for at least the reasons set forth in pages 7 and 8 in Applicant's Response filed on February 8, 2007.

Dependent Claims 2-9 and 21

Each of claims 2-9 and 21 incorporates the features of independent claim 1 and therefore is patentable over Hideshima and Wu for at least the same reasons explained above. Claims 8 and 9 also

are patentable over Hideshima and Wu for the additional reasons set forth on pages 8 and 9 in Applicant's Response filed on February 8, 2007.

Claims 1-4 and 6-11

Claims 1-4 and 6-11 are rejected under 35 U.S.C. § 103(a) over Hideshima (U.S. 5,143,865) in view of Kunikiyo (U.S. 6,717,267). In the rejection of independent claim 1, the Examiner has stated that Hideshima "does not disclose a top side thermal dissipation metallization" (see page 4, ¶ 14, lines 5-6, of the Office Action dated May 7, 2007). In an effort to make-up for this failure of Hideshima's disclosure, the Examiner has relied on the teachings of Kunikiyo. In particular, the Examiner has taken the position that (see page 4, ¶ 14, lines 6-11, of the Office Action dated May 7, 2007):

> . . . Nevertheless, Kunikiyo (e.g. fig. 19) shows a top side thermal dissipation metallization 31. According to Kunikiyo, this type of mounting structure provides more satisfactory effect of cooling away the heat in the interlayer insulating films than conventional semiconductor devices having no dummy interconnections or dummy plugs, since metal has higher thermal conducting rate than the interlayer insulating films. This improves the circuit operation of the semiconductor device (col. 23/lls. 1-18) ....

In FIG. 19, Kunikiyo discloses a semiconductor device that includes dummy interconnections 9a-b, 21a-c, and 25a-c, dummy plugs 22a-b, 26a-c, 29b-c, and 31, and a heat sink 32. The dummy interconnections are formed in order to improve the flatness in the CMP processes used in the formation of the semiconductor device and to correct the proximity effect in which the finished resist form is affected by the proximate pattern form in the transfer processes used in the formation of the semiconductor device (see, e.g., col. 5, lines 46-50). The dummy plugs 22a-b, 26a-c, and 29b-c serve to connect the dummy interconnections to ground potential in order to reduce noise (see, e.g., col. 10, lines 28-38). The dummy plugs 31 serve to transfer heat from the interlayer insulating films to the heat sink 32, which dissipates the heat.

Contrary to the Examiner's statement, the dummy plugs 31 do not constitute a "thermal dissipation metallization."

First, the dummy plugs 31 do not constitute a "metallization" as defined in the specification. On page 4, lines 3-4, the specification of the instant application recites that "As used herein, the term "metallization" refers to single-layer metal film or a multi-layer metal film formed in or on an integrated circuit." The dummy plugs 31 do not constitute a single-layer metal film or a multi-layer metal film. Instead, the dummy plugs 31 constitute a small number of spaced apart metal plugs that are positioned only where the dummy interconnections are located and are formed by filling through holes in the passivation film 30 with metal and chemically-mechanically removing excess metal until the top surfaces of the plugs 31 and the passivation film 30 coincide (see, e.g., FIG. 19 and col. 11, line 36 - col. 12, line 23).

Second, the dummy plugs 31 do not constitute a "thermal dissipation" metallization in

accordance with the ordinary and accustomed meaning of the term "thermal dissipation." In accordance with its ordinary and accustomed meaning, the word "dissipation" refers to the action or process of breaking up and driving off or causing to spread thin or scatter and gradually vanish (see, e.g., Merriam-Webster's Collegiate Dictionary, 10th Ed.). The word "thermal" means "of, relating to, or caused by heat" (see, e.g., Merriam-Webster's Collegiate Dictionary, 10th Ed.). The dummy plugs 31 do not break up and drive off heat nor do they cause heat to spread thin or scatter and gradually vanish. Instead, the dummy plugs 31 merely conduct heat from the regions of the interlayer insulating films near the dummy interconnections to the heat sink 32, which dissipates the heat.

Thus, one skilled in the art at the time the invention was made reasonably would not have considered the dummy plugs 31 to be a "thermal dissipation metallization" as recited in claim 1. Since neither Hideshima nor Kunikiyo teaches or suggests anything about a die that has a top side supporting top side thermal dissipation metallization as recited in claim 1, the combination of Hideshima and Kunikiyo cannot possibly teach or suggest the invention defined by independent claim 1. For at least this reason, the Examiner's rejection of independent claim 1 under 35 U.S .C. § 103 (a) over Hideshima and Kunikiyo should be withdrawn.

The rejection of claim 1 under 35 U.S.C. § 103(a) over Hideshima in view of Kunikiyo also should be withdrawn because this rejection relies on an impermissible combination of the teachings of Hideshima and Kunikiyo.

The Examiner has stated that (see page 4, ¶ 14, lines 12- 16, of the Office Action dated May 7, 2007):

> . . . It would have been obvious to one of ordinary skill in the art at the time the invention was made to include in Hideshima's invention a topside thermal dissipation metallization such as dummy patterns in accordance to Kunikiyo's invention to improve the circuit operation since the heat can be satisfactorily removed form the interlayer insulating films.

This rationale, however, does not establish a *prima facie* case of obviousness under 35 U.S.C. § 103 (see MPEP § 706.02(j)) for at least the reasons set forth on pages 11 and 12 in Applicant's Response filed on February 8, 2007.

Dependent Claims 2-4 and 6-11

Each of claims 2-4 and 6-11 incorporates the features of independent claim 1 and therefore are patentable over Hideshima and Kunikiyo for at least the same reasons explained above. Claims 8-11 also are patentable over Hideshima and Kunikiyo for the additional reasons set forth on page 13 in Applicant's Response filed on February 8, 2007.

Dependent claims 12 and 13

Claims 12 and 13 are rejected under 35 U.S.C. § 103(a) over Hideshima, Kunikiyo, and Wang (US. 5,977,626). Each of claims 12 and 13 incorporates the features of claim 10. Claims 12 and 13 also are patentable over Hideshima, Kunikiyo, and Wang for the additional reasons set forth

on page 14 in Applicant's Response filed on February 8, 2007.

Dependent claim 14

Claim 14 is rejected under 35 U.S.C. § 103(a) over Hideshima, Kunikiyo, and Khan (U.S. 6,853,070). Claim 14 incorporates the features of independent claim 10. Claim 14 is also patentable over Hideshima, Kunikiyo, and Khan for the additional reasons set forth on page 14 in Applicant's Response filed on February 8, 2007.

Claims 15-18

Claims 15-18 are rejected under 35 U.S.C. § 103(a) over Hideshima in view of White (U.S. 5,665,655) and Kunikiyo. Independent claim 15 recites features that essentially track the pertinent features discussed above in connection with independent claim 1. White does not make-up for the failure of Hideshima and Kunikiyo to teach or suggest the pertinent features of independent claim 1 discussed above. Indeed, the Examiner merely has cited White for showing "a method including the step of forming multiple die regions on a substrate and the step of . . . singulating the die regions to form the integrated circuit . . . [dice] ." Moreover, the proposed combination fails to disclose, teach or suggest at least "forming on a top side of a substrate ... an exposed top side thermal dissipation metallization," Therefore, claim 15 is patentable over Hideshima in view of White and Kunikiyo for at least the same reasons explained above in connection with independent claim 1.

Dependent claims 16-18

Each of claims 16-18 incorporates the features of independent claim 15 and therefore is patentable over Hideshima, White, and Kunikiyo for at least the same reasons explained above. Claim 18 also is patentable over Hideshima, White, and Kunikiyo for the additional reasons set forth on page 16 in Applicant's Response filed on February 8, 2007.

Dependent claims 19 and 20

Claims 19 and 20 are rejected under 35 U.S.C. § 103(a) over Hideshima in view of White, Kunikiyo, and Wang. Each of claims 19 and 20 incorporates the features of claim 18 and claim 15. Claims 19 and 20 also are patentable over Hideshima, White, Kunikiyo, and Wang for the additional reasons set forth on page 16 in Applicant's Response filed on February 8, 2007.

Conclusion

For the reasons explained above, all of the pending claims are now in condition for allowance and should be allowed. Charge any excess fees or apply any credits to Deposit Account No. 50-3718.

Respectfully submitted,

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